Gator: Toward a Correct Technology Mapper

A talk from your pal Andrew!!!

yeah!!!!!!

Hardware Compilation

First, what does a software compiler do?

```
// TODO @(bsaiki): andrew, do we need this?
int add_some_stuff() {
   a = 1;
   b = 2;
   c = 3;
   return (a + b) & c;
}
```

High-level **source code**

→

```
movq %rdi, $1
movq %rsi, $2
movq %rdx, $3
addq %rdi, %rsi
andq %rax, %rdx
```

Low-level implementation,
expressed as a series of **assembly instructions**

Hardware Compilation

What does a hardware compiler do?

```
module my_design
  (input a,
   input b,
   input c,
   output out);
  assign out = (a + b) & c;
endmodule
```

High-level **design fragment**

→

```
module my_design
  (input a,
   input b,
   input c,
   output out);
   wire mid;
   adder a0(.a = a, .b = b, .o = mid);
   ander a1(.a = mid, .b = c, .o = out);
endmodule
```

Low-level implementation,
expressed as
hardware primitives

Hardware Compilation

What does a hardware compiler do?

```
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  (input a,
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```
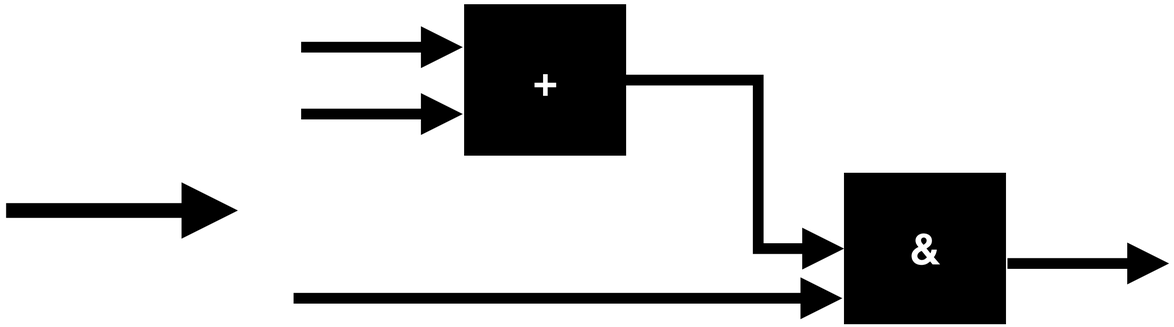



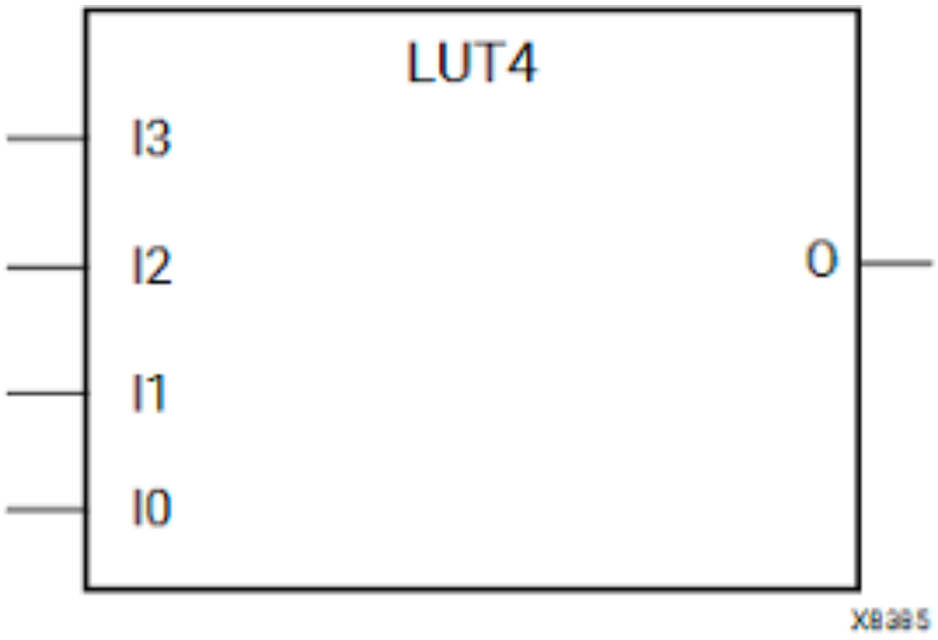
High-level **design fragment**

Low-level implementation,
expressed as
a picture on a rock

Primitives are complex!

LUT4

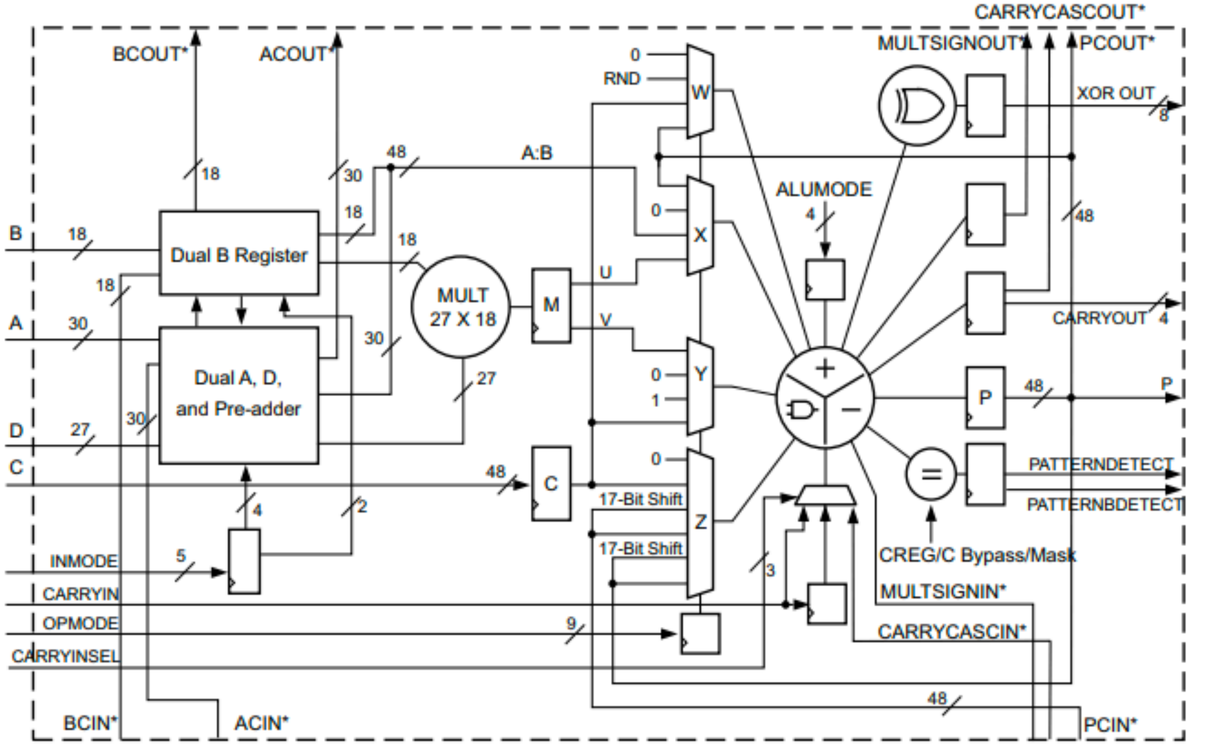
- 4-bit truth table
- Has state: internal memory



Primitives are complex!

DSP48E2

- Common use cases:
  - barrel shifting
  - SIMD operations
  - `(a + b) * c & d`
- Can be pipelined for 3 cycles



*These signals are dedicated routing paths internal to the DSP48E2 column. They are not accessible via general-purpose routing resources.

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Primitives are complex!

What can the DSP48E2 actually do?

increase in challenge for technology mappers [6]. The UltraScale+ DSP48E2 has over 100 ports and parameters, and the manual that explains how to configure them properly is over 75 pages long [10]. The large number of ports and parameters is due to the fact that these primitives

What does it mean for a primitive to be correct?

How do we know a DSP configuration is correct?

- If the DSP is configured correctly, then for some time t, it should:
  - compute the correct result on time t, which is true if
  - it had correct state on time (t - 1), which is true if:
  - it had correct state on time (t - 2), which is true if:
  - it had correct state on time (t - 3), which is true if:
  - ... shoot!

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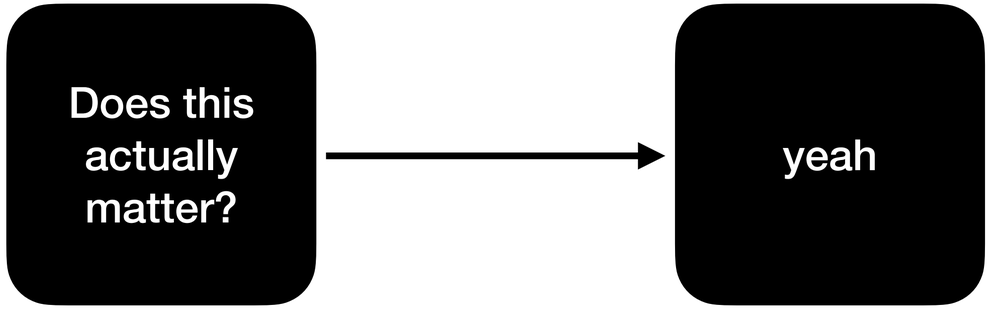
Solution from Vivado: don't provide these correctness guarantees!

Do correctness guarantees actually matter?

Verified Compilation in Software

Does this actually matter?

Verified Compilation in Software



Finding and Understanding Bugs in C Compilers

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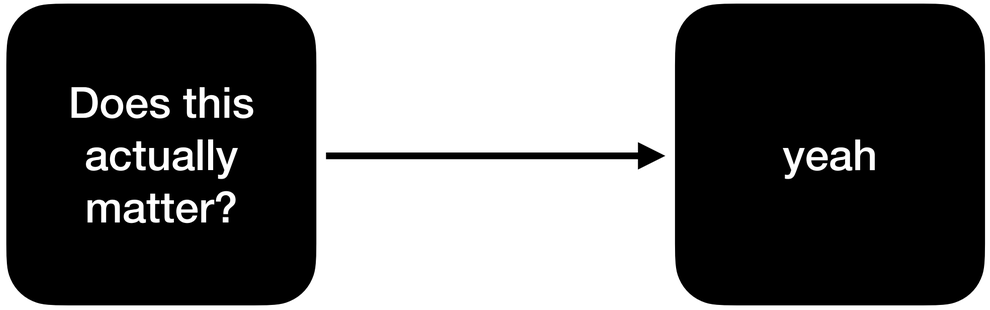
Verified Compilation in Software

Verified Compilation in Hardware

Does this actually matter?

Verified Compilation in Hardware



Finding and Understanding Bugs in FPGA Synthesis Tools

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Verified Compilation in Hardware

Formally Verified Hardware Compilation

Lutsig: A Verified Verilog Compiler for Verified Circuit Development

Andreas Lööw
Chalmers University of Technology
Gothenburg, Sweden

Formally Verified Hardware Compilation

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"Lutsig's technology mapped output netlists for this class of FPGAs contain <u>only k-LUT (with k ≤ 6) and carry4 cells</u>"

Formally Verified Hardware Compilation

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What about my DSP!? 🤬

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About

Verilog development and verification project for HOL4

hardware | verilog | synthesis | formal-methods | formal-verification | hol

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acjf3

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If a hardware compiler is **extensible,** support for additional primitives can be added with little user effort.

If a hardware compiler is **extensible,** support for additional primitives can be added with little user effort.

In general, hardware compilers aren't extensible!

Lakeroad: an extensible compilation tool

- Lakeroad uses **program synthesis** to map high-level designs to low-level **hardware primitives**.
- Lakeroad reasons about what a primitive can do through **automatic extraction of SMT semantics** from **vendor-provided simulation models.**

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  - Write a short sketch

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- Lakeroad uses **program synthesis** to map high-level designs to low-level **hardware primitives**.
- Lakeroad reasons about what a primitive can do through **automatic extraction of SMT semantics** from **vendor-provided simulation models**.
- What does the workflow of Lakeroad actually look like?

Lakeroad's Compilation Flow

```
(a + b)
```

ALU

1. Download the simulation model

```
(a + b)
```

ALU

ALU.v

1. Download the simulation model

```
(a + b)
```

ALU

I can add and multiply!

ALU.v

1. Download the simulation model

```
(a + b)
```

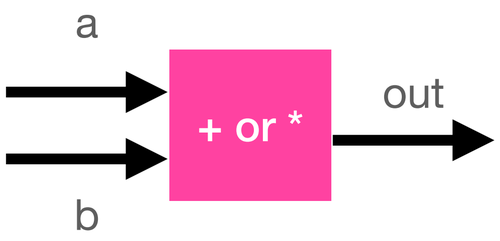
+ or *

I can add and multiply!

ALU.v

2. Set up a sketch

```
(a + b)
```



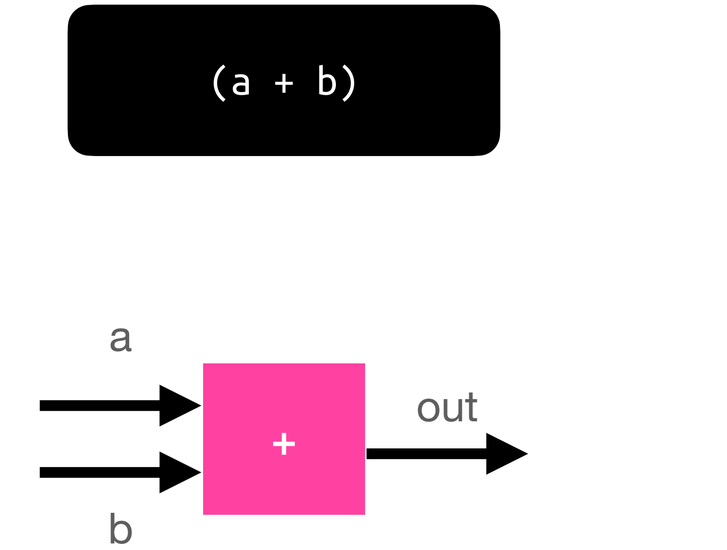
ALU.v

3. Lakeroad's synthesis query:

```
def impl(a, b, t):
   return a + b

def sketch(a, b, t):
  return a (+ or *) b

assert (forall a, b,
  impl(a, b, 1) == sketch(a, b, 1) and
  impl(a, b, 2) == sketch(a, b, 2)
```



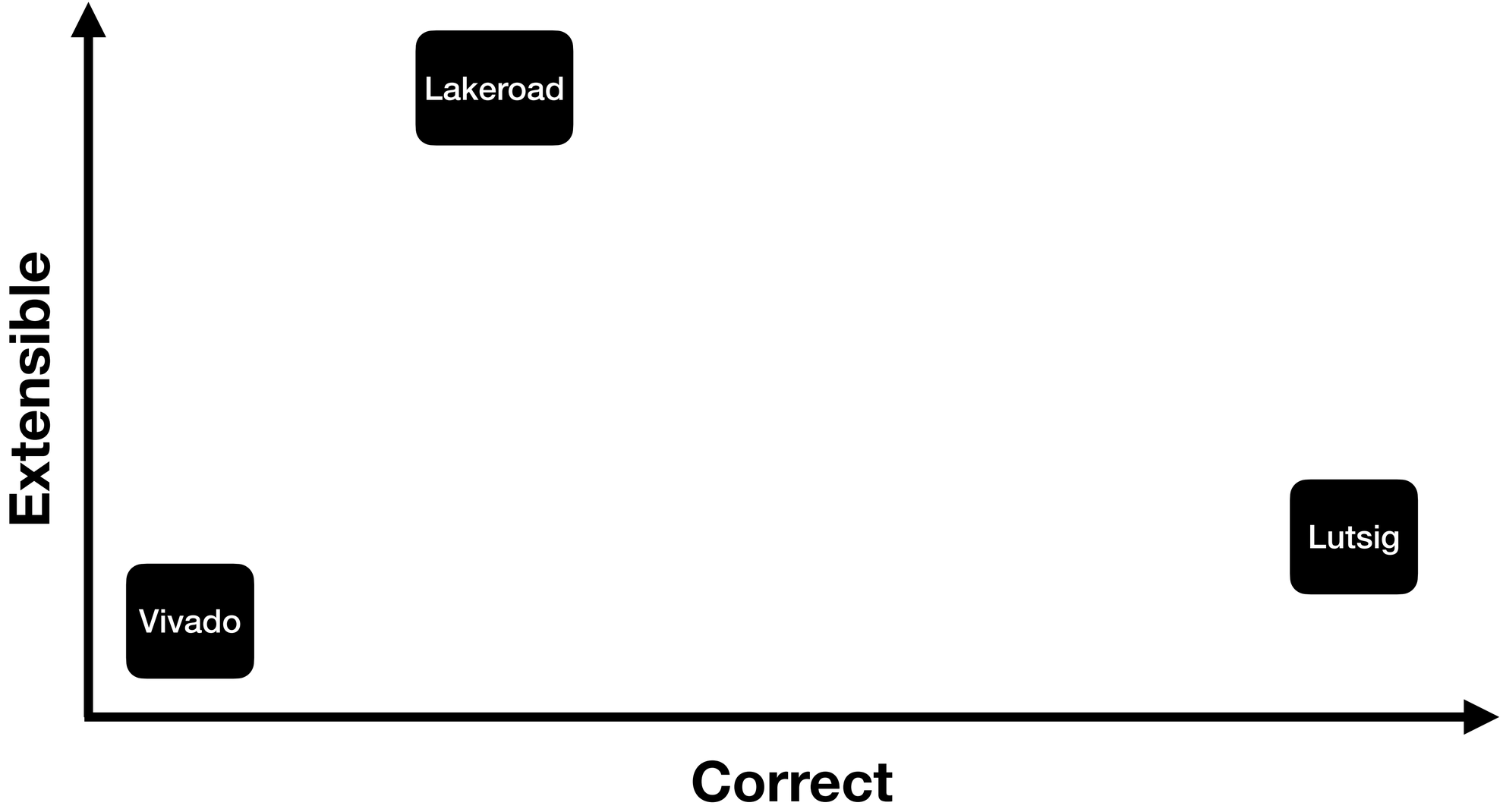
ALU.v

Lakeroad's correctness guarantees

- Lakeroad's program synthesis query does a **"bounded model synthesis"** where correctness for the first few cycles is formally guaranteed.
- ...but this doesn't account for all the other cycles!
- Lakeroad provides **some guarantees** for correctness, but not **full** guarantees.

```
assert (forall a, b,
  impl(a, b, 1) == sketch(a, b, 1) and
  impl(a, b, 2) == sketch(a, b, 2)
```

A Survey of Hardware Compilers



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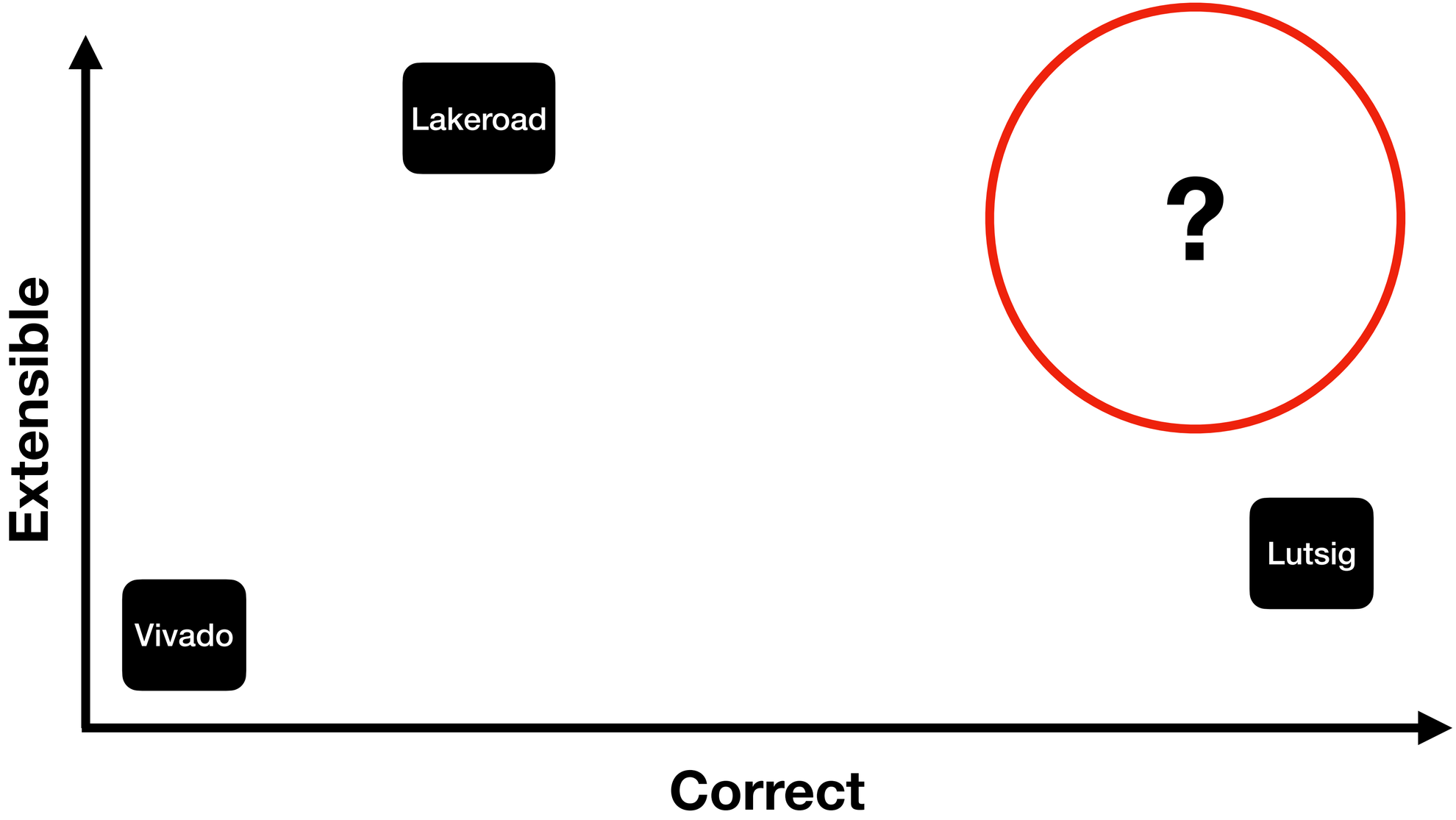

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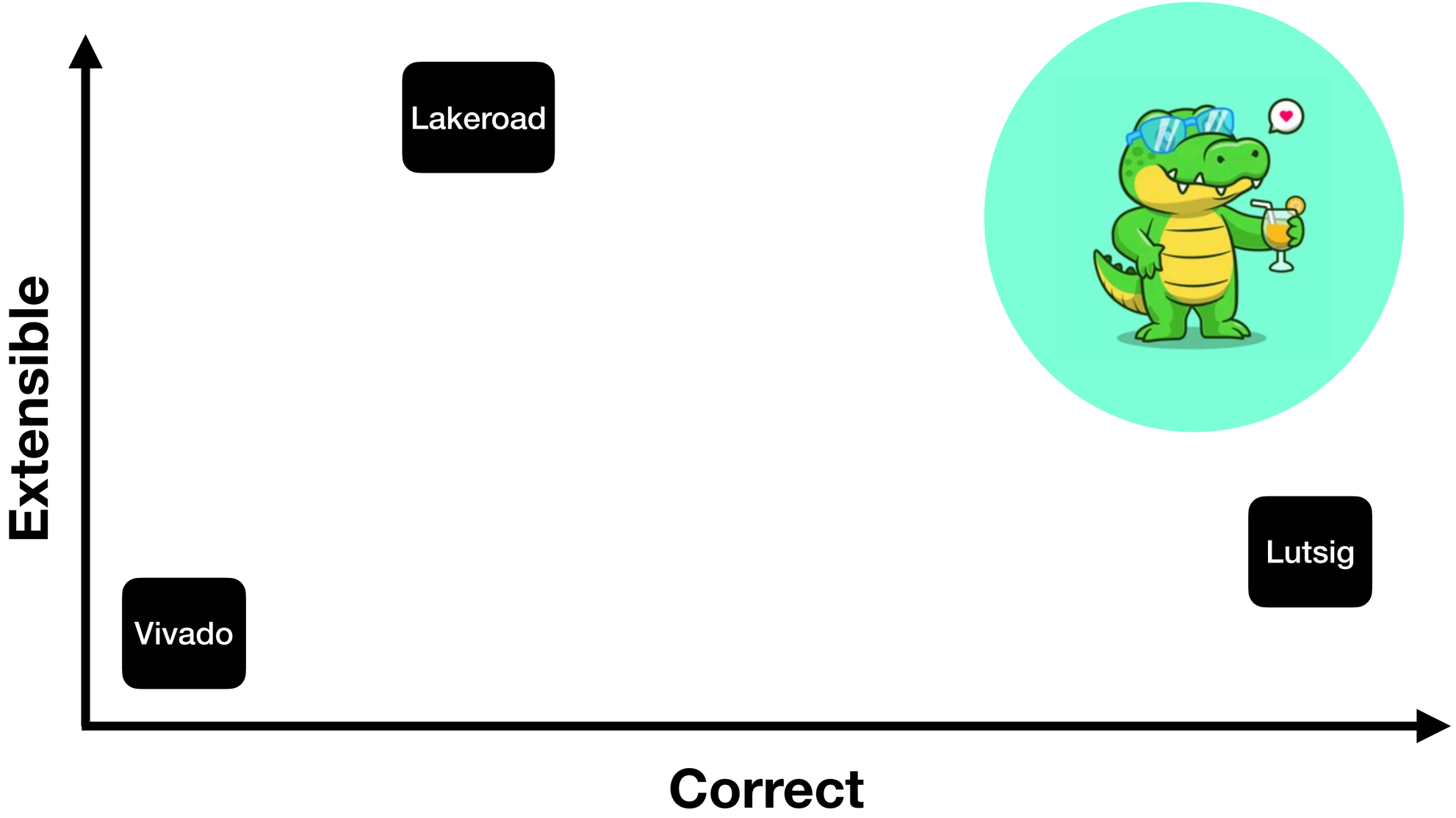

🐊 The Gator™ Project™ ©:

- Goal: a hardware compiler which is **correct** and **extensible.**
- What if we modify Lakeroad's synthesis query so that it's correct **for all time?**

$$\forall i : spec(i,1) = impl(i,1) \wedge spec(i,2) = impl(i,2)$$

$$\Downarrow$$

$$\forall i, t : t > init \rightarrow spec(i,t) = impl(i,t)$$

Demo Time! (maybe)

Thank you!!